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This technical report has been reviewed and is approved for publication.

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REPORT SUMMARY

MCT layers have been grown by MOCVD on CdTe, GaAs and GaAs/Si for device processing. Both (111) and (100)MCT have been grown on GaAs and the relative merits of the two orientations are discussed. The effects of the substrate preparation, pre-bake, nucleation and buffer growth on the final MCT layer are dicussed. Optimisation of the growth conditions led to (100)MCT layers being p-type as grown with FWHM's of 80-90 arc seconds.

CdTe has been grown on (311)A and B GaAs. The CdTe adopts one of several orientations [(110) or 3-4° (311)] and is untwinned with a relatively smooth surface morphology. Continuing studies of CdTe growth on Si indicate that the nucleation temperature should be higher than 450°C.

Annealing studies have been carried out to establish material of a consistent p-type carrier concentration for processing, and to understand the diffusion mechanism within the material. A reproducible p-type anneal has been established.

Linear arrays of LWIR and MWIR diodes have been formed in MCT/GaAs by diffusion through a ZnS mask. Typical 77K detectivities of 1.5×10^{11} cmHz$^{1/2}$W and 1.1×10^{11} cmHz$^{1/2}$/W have been obtained at 77K for 5.5 and 11 μm cut-off diodes respectively, with quantum efficiencies greater than 70%.

77K R_0A products obtained over a range of cut-off wavelengths are comparable to the state-of-the-art literature values. R_0A's of 10 Ωcm^2 have been obtained for arrays with a 11 μm cut-off.

DARPA PROJECT F49620-88-C-0059:

Integrated Technology in Mercury Cadmium Telluride on Gallium Arsenide and Mercury Cadmium Telluride on Silicon for Medium and Long Wavelength Infra-red Detector Arrays.

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INTEGRATED TECHNOLOGY IN MERCURY CADMIUM TELLURIDE ON GALLIUM ARSENIDE AND MERCURY CADMIUM TELLURIDE ON SILICON FOR MEDIUM AND LONG WAVELENGTH INFRA-RED DETECTOR ARRAYS

This is the final report on Project F49620-88-C-0059. It covers growth studies and diode fabrication in MCT/CdTe, MCT/GaAs and MCT/GaAs/Si. The layers were grown at GEC, UK, and were processed at SAT, France, Initially the wafers were processed as-grown, but during the course of the project the importance of annealing to achieve a consistent carrier concentration before p-n junction formation was realised.

The report has been divided into growth, and annealing and photodiode processing sections.

1 GROWTH STUDIES

The MCT layers were grown by the IMP process [1,2] in an experimental MOCVD system [3]. The MCT was grown at 350°C from diisopropyltelluride (DIPT) and dimethylcadmium (DMCd) supplied by Epichem Ltd, and elemental mercury from Cominco. The partial pressures of DIPT and DMCd were about 1×10^{-4} atm.

Fourier transform infrared spectroscopy (FTIR) was used to map the thickness and composition of the MCT layers. The thicknesses of HgTe and CdTe films were estimated from calibrated photomicrographs of the cleaved layers.

Electrical characteristics were determined using Hall effect measurements over the temperature range 10-300K at magnetic fields of 0.1-0.6T.

In the case of the samples with highly conducting HgTe buffer layers, these dominated the Hall measurements and also prevented the determination of composition by infrared transmission measurements.

A GaAs crystal was used as the first crystal for the double crystal X-ray diffraction measurements [(004) and (333) CuKβ reflections for analysis of the (100) and (111) samples respectively].

1.1 Growth on CdTe

Until recently the highest quality photodiodes had been produced in epitaxial MCT/CdTe and related compounds (Cd,Zn,Te,Se), so layers were grown on CdTe to provide a baseline for the diode fabrication. These II-VI substrates have the advantage of a good lattice match to MCT, but are expensive, fragile and are not available in large areas at a reasonable cost. There is no possibility of integrating readout and sensor circuitry on these substrates in the foreseeable future.

1.1.1 Results and discussion

The layers sent to SAT for device processing were reported in the last year's annual report and are summarised in Table 1. Good LWIR diodes were made in (111)MCT/CdTe, but half of the layers supplied to SAT (including all the (100)MCT wafers) were considered too small (10 x 15 mm^2) to process. The (100)MCT layers were used for annealing studies, though the

presence of a thin HgTe buffer layer (used successfully to improve the surface morphology) complicated the interpretation of the results (see Section 2).

No further growth and diode fabrication was done on MCT/CdTe this year. The substrates available at reasonable cost were considered too small for processing, and the main thrust of the project was to grow on GaAs, Si or GaAs/Si: consequently the effort this year was directed into growth on these substrates.

1.2 The growth on GaAs

The following systems were studied:

(1) (100)MCT/buffer/(100)GaAs
(2) (111)MCT/CdTe/(111)B GaAs
(3) (111)MCT/(111)CdTe/(100)GaAs
(4) CdTe/(311)A and B GaAs

The relative merits of these systems were discussed in the first year's annual report. The (100) orientation suffers from hillocks which are believed to be generated at the substrate/buffer interface [4,5]. The areas between these hillocks are of better crystallinity than the (111) orientation, and are not twinned. The (111) orientation is usually twinned but has a smooth surface morphology which is suitable for device fabrication.

CdTe and MCT grown on (311) and (211) GaAs have been reported as being untwinned with a smooth surface morphology [6,7,8], and CdTe growth on (311)A and B GaAs has been investigated.

1.2.1 Results and discussion

The growth sequence for MCT/GaAs consisted of the following stages: (a) substrate preparation; (b) pre-bake of substrate in the reactor; (c) nucleation of CdTe; (d) buffer layer growth; (e) MCT growth; (f) cool down. Each of these stages is discussed in detail below.

(a) Substrate preparation prior to growth

Czochralski grown (111)B and 2°(100) (towards the nearest <110>) GaAs substrates were supplied by Mi-Net Technology. The wafers were semi-insulating with an etch pit density (EPD) of less than 50,000/cm^2. (311)A and B GaAs substrates were supplied by Cambridge University.

An etch of the substrate would remove any surface damage and temporarily remove oxides, but might accentuate or generate defects.

The use of a sulphuric acid or ammonia based etch was investigated, as was the effect of no etch at all.

(b) Pre-bake prior to growth

A bake at about 580°C for ten minutes is required to remove gallium oxide from the GaAs, but the surface will be degraded at temperatures greater than 450°C because of arsenic loss. The effect of the pre-bake on the final MCT layer was investigated.

(c) Nucleation of CdTe for (100) growth

Epitaxial MCT cannot be grown directly onto GaAs, so CdTe is used as the nucleation layer. A low temperature nucleation has been shown to be important to establish the (100) orientation [9]. The nucleation temperature was investigated, as was the effect of a short bake on the CdTe layer to try to anneal out dislocations. (111)CdTe layers were nucleated at the growth temperature so this step is not discussed separately for this orientation.

(d) Buffer growth

This is required to accommodate misfit dislocations generated at the substrate interface and to contain any out-diffusion of gallium.

CdTe was used as the buffer for (111)MCT growth, and high x MCT, CdTe or combinations of CdTe and HgTe layers were used for (100)MCT. The effect of varying the cadmium to tellurium ratio on the crystallinity and photoluminescence of the CdTe buffer was reported earlier [8]. It was

found that a 1:1 ratio was best for a good surface morphology and crystallinity. The effect of a short bake of the CdTe buffer to anneal out dislocations was investigated.

(e) MCT growth

The susceptor and mercury zone temperatures were selected to give a reasonably high growth rate whilst minimising pre-nucleation. The effect of a long anneal under growth conditions on the crystallinity of the MCT layer was investigated.

(f) Cool down

The cool down conditions are important since the MCT could be given an unintentional anneal during this process, which might change the number of mercury vacancies and thus affect the majority carrier concentration and type.

1.2.2 Conclusions

(a) Substrate preparation prior to growth

(i) Good quality p-type (100) layers could be grown on un-etched (100)GaAs. Consequently no etch was used for the (100)MCT growth.

(ii) (111)MCT could be grown via CdTe on (111)GaAs without an etch. Consequently no etch was used for (111)MCT growth on (111)GaAs.

(iii) An etch was necessary to obtain (111)MCT/(100)GaAs.

(iv) The sulphuric acid based etch (H_2SO_4:H_2O_2:H_2O,5:1:1) tended to produce pits and the temperature was crucial. Consequently the ammonia based etch was used (NH_4OH:H_2O_2:H_2O,5:1:5). The quality of the DI water is critical, and a long final DI rinse was required (at least 1 hour for the sulphuric acid based etch).

(b) Pre-bake prior to growth

(i) A long high temperature pre-bake (e.g. 30 minutes at 610°C) did not seem to have a detrimental effect on the (100)MCT layers in terms of crystallinity and facet density. See Table 2 - layers 1252 (1) and (2).

(ii) Mixed orientation (i.e. both (100) and (111)) layers were obtained on (100)GaAs if no pre-bake (and no etch) were used (see Table 2 - layer 1256 (1)).

(c) Nucleation for (100) growth

(i) Low growth rates (of less than 1 μm/hr) were needed to establish the (100) orientation. 310°C appeared to be the critical temperature (see Table 2 - layer 1264 (1)) and a temperature of 300°C was eventually selected.

(ii) The length of the nucleation (5-60 minutes) did not have any effect on the surface morphology or crystallinity (see Table 2).

(iii) A short anneal of the nucleation layer (430°C for 10 minutes) did not appear to improve the crystallinity (see Table 2 - layer 1252 (1) and (2)).

(d) Buffer growth

(i) Only 0.5 - 1 μm CdTe was necessary to contain the out-diffusion of gallium, under the growth temperature and conditions, chosen for the (100) and (111) orientations. This was shown by SIMS and was reported in last year's annual report.

(ii) Layers with thin CdTe buffers (~2.5 μm) appeared to show better crystallinity for (100)MCT. The best values were 80-90 arc seconds. See Table 2 - layers 1257 (1), 1263 (1).

(iii) A short anneal of the CdTe buffer (430°C for 10 minutes) did not improve the crystallinity (see Table 2 - layer 1252 (1) and (2)).

(iv) Various different types of buffer were tried to reduce the facet density of (100)MCT/(100)GaAs. Combinations of HgTe and CdTe layers were used successfully, leading to low facet density layers (30-100/cm^2) over large areas whilst maintaining the crystallinity [9]. Details are given in last year's annual report.

(e) MCT growth

The susceptor and mercury zone temperatures were chosen to give reasonable growth rates (10-20 μm/hr) whilst minimising pre-nucleation of CdTe.

Initially, layers for processing were grown about 10 μm thick, and these layers exhibited mixed conduction (as grown).

The thickness of the layers was increased at the request of SAT, and the thicker layers were typically p-type as grown, $5 \times 10^{16}/cm^3$, μ = 250-750 cm^2/Vs.

It has been reported that the ten minute anneal at the end of the IMP growth was too short, and that it should be increased to one hour [10], and so the length of this post-growth anneal was investigated. The longer anneal improved the crystallinity of the thinner layers, but even with the short anneal the thicker layers had equally good crystallinity (see Table 2 - layers 1260 (1), 1261 (1)). The improvement in epitaxial material quality with increased thickness is well known [11,12].

Some preliminary work on the length of the post-growth anneal was reported in the DARPA quarterly technical report 1/3/89-31/5/89. A thinner layer (8 μm) showed an improvement in crystallinity after a long anneal under growth conditions.

(f) Cool down

The mercury zone was always cooled faster than the susceptor to avoid any unintentional indiffusion during this stage. It has been suggested that (111) layers may be p-type after growth, but show mixed conduction after the cool down [13]. Tables 3 and 4 summarise all the MCT/GaAs layers that were sent to SAT.

1.2.3 Growth on (311)A and B GaAs

Preliminary work on CdTe growth on (311)GaAs was reported in the QTR 1/6/89-31/8/89. (110)CdTe was grown on (311)B GaAs, untwinned with a smooth surface morphology [8]. The layer was nucleated at the growth temperature (370°C). It has been suggested that the (311) surface is closer to the (100) than the (111) surface in terms of dangling bonds [14,15]. Consequently some work was undertaken with a low temperature nucleation. The use of different etches/no etch has also been studied.

1.2.3.1 Results and discussion

CdTe was grown on both (311)A and B GaAs under a variety of temperatures and nucleation conditions. The etches used were as described for the (100) and (111)GaAs (Section 1.2.1(a)) and it was found that the NH_4OH based etch was not suitable, and more work is needed to optimise the etch.

Various surface morphologies have been observed (see Figure 1) though these were indistinguishable crystallographically. Laué photography

showed that both (110) and 3-4°(311)CdTe oriented layers have been obtained. These preliminary investigations show that growth on (311)GaAs is complex but promising.

1.3 Growth on GaAs/Si

The advantages of growth on GaAs/Si were outlined in the first year's annual report. The (100)GaAs/(100)Si wafers (grown by MOCVD) were supplied by Kopin Corporation. The epilayers are of poorer quality than bulk GaAs, in terms of the crystallinity (190 arc seconds wrt 18 arc seconds) and the defect density.

The same growth sequence was used as for growth on bulk GaAs, but more care was taken during the etch since the GaAs layer was only 2.5 μm thick.

1.3.1 Results and discussion

In general the (100) layers on (100)GaAs/Si had a higher hillock density than those on (100)GaAs.

Two layers were submitted to SAT for device fabrication. The layers were (100)MCT/(100)CdTe/(100)GaAs/(100)Si. The layers sent were:

1180 = 18 μm x = 0.206 (±0.001)MCT/3 μm CdTe/GaAs/Si. The layer exhibited mixed conduction Hall characteristics.

1297 = 18 μm, x = 0.254 (±0.011)MCT/2 μm CdTe/GaAs/Si. The layer exhibited mixed conduction Hall characteristics, with a FWHM of 112-119 arc seconds.

1.4 Growth on Si

Most of the work of CdTe nucleation on Si was detailed in last year's annual report. The major part of the work this year was postponed because of problems with high total oxidisable carbon (TOC) levels in the DI water.

1.4.1 Results and discussion

A study of CdTe layers on (001), 2°(001), (111) and 2°(111)Si grown at 290°C, 350°C and 450°C was undertaken using TEM and RHEED. Different silicon cleaning techniques were discussed in the first year's annual report. The substrates were given a 10s dip in HF, then a 10 minute ultra violet ozone 'UVOC' clean (16). All the films were polycrystalline, with grain size increasing with temperature, and no preferred texture/orientation relationships to the substrate. The average grain size on the CdTe grown on (001)Si was found to be slightly larger than that grown on the 2°(001)Si, whereas no appreciable difference in the grain size was seen between the CdTe on (111) and 2°(111)Si.

1.4.2 Conclusions

Results from this year indicate that the nucleation temperature should be higher than 450°C. Improvements in the DI water system have re-opened this area for future research.

2 DIODE FABRICATION

MOCVD layers grown on GaAs and GaAs/Si have been processed at SAT, Poiters, France. SAT have a well-developed diode process for THM material but have found that some of the MOCVD material behaves very differently when processed. In the first year the wafers were processed as-grown, regardless of carrier concentration and type, which added some uncertainty to the interpretation of results. As the process uses mercury diffusion to form n on p diodes, it was necessary to optimise annealing conditions for both n to p and p to n. Optimisation of the "p anneal" was essential to obtain wafers of a consistent p-type carrier concentration as a starting material. Optimisation of the "n anneal" (Hg diffusion) was needed to obtain the correct junction depth and n-region carrier concentration.

2.1 Annealing studies

2.1.1 p-type anneal

MCT layers that showed mixed conductivity as grown (all the (111) layers and some of the (100) layers) needed to be annealed to p-type

(~5 x $10^{16}/cm^3$) with a mobility of approximately 300 cm^2/Vs before processing. The reason these layers show mixed conduction after growth is not fully understood. It has been suggested that the layers may be p-type but start to anneal to n-type during the cool down after growth [13]. Another explanation could be that a high dislocation density is set up at the interface, and interface effects cause the mixed conduction.

The experiments performed on sample 1114 (MCT grown on (100)GaAs with a buffer structure containing a HgTe layer) and 1296 (MCT grown on (111)GaAs with CdTe buffer) show that annealing at 300°C under vacuum for 2 hours converts the samples from anomalous conduction to p-type with a carrier concentration ranging from 2-4 x $10^{16}/cm^3$, see Tables 5 and 6. Annealing temperatures higher than 300°C tended to cause deterioration of the surface morphology.

Samples 1181 and 1184 (both containing CdTe/HgTe buffers) were not converted to p-type after the 2 hour, 300°C vacuum anneal, nor after increasing the duration to 6 hours, see Tables 7 and 8. These layers were grown with buffer structures containing a HgTe layer which in some cases dominates the as-grown Hall measurements and may explain these inconsistent results.

Optimisation of growth conditions meant that the (100) layers were p-type as grown so this step was unnecessary.

2.1.2 n-type anneal

The photodiode p-n junction is formed by a local p to n anneal through windows in a ZnS layer. It is expected that under optimised conditions the depth of the p to n conversion would depend on the duration of the anneal. Complete conversion of p to n-type was investigated, as Hall measurements would provide insight into the quality of the n regions of the diodes formed by diffusion. It would be expected that layers that annealed easily and reproducibly would be good samples for processing. A difference was observed between the (100) and (111) orientations, as illustrated below.

1257 (100)MCT/(100)CdTe/GaAs

This sample was p-type as grown and showed mixed conduction after heat treatment in a mercury-rich atmosphere at 310°C for 2 hours or 210°C for 6 days, see Table 9. The decrease in mobility with increasing Hall field shows that the conversion is not complete and the mobility is lower than expected for this composition (x ~0.22).

1296 (111)MCT/CdTe/GaAs

This sample showed mixed conduction as grown, but annealed to p-type by the p anneal schedule, see Table 6. However it reverted to mixed conduction after 3 hours at 310°C in a mercury atmosphere. A further anneal of 27 hours under the same conditions did not convert the sample to n type.

2.1.3 Conclusions

Both the (100) and (111)MCT layers could be annealed reproducibly to p-type. n annealed layers show mixed conduction and therefore the conditions for this anneal have not yet been optimised. Further work is necessary to establish the n-annealing conditions.

2.2 Photodiode processing

The detector geometry was a linear array of 60 x 100 μm^2 or 30 x 30 μm^2 sensitive areas formed by mercury diffusion.

The process was then as follows:

(i) p-type anneal from mixed conduction to p ($\sim 5 \times 10^{16}/cm^3$) carrier concentration, if necessary.

(ii) **Surface preparation.** The sample was lightly etched in a 1% Br/MeOH solution to remove about 0.5 μm. This was followed by solvent and DI rinses.

(iii) **Deposition of dielectric and masking layers.** A layer of CdTe 0.25 μm thick was sputtered onto the layer. A ZnS layer of 0.75 μm thickness was then sputtered and diffusion windows were opened in the ZnS.

(iv) **Ion implantation.** Following results obtained last year, which showed that the diodes had anomalously small sensitive area, an ion implantation step has been added to the standard process. This involves an implantation of donor atoms through the diffusion window to create a low resistance n^+ surface and improve the collection efficiency over the area of the diode. It has been established that this step does not in itself form the p-n junction (see section 2.2.2).

(v) **Mercury diffusion.** The layers were annealed at 300°C under saturated mercury vapour conditions to produce n-type regions in the p-type layer corresponding to the windows in the ZnS coating.

(vi) **Passivation.** The ZnS mask was then removed and passivating layers of CdTe and ZnS were sputtered (0.15 μm of CdTe and 0.5 μm of ZnS).

(vii) **Electrical contacts.** The CdTe and ZnS coatings were etched to reveal the n and p regions and electrical contact pads were made by sputtering Cr/Au.

A schematic diagram of the diode structure is shown in Figure 2. The diode arrays normally consist of greater than 100 elements.

2.2.1 Characterisation techniques

The following techniques have been used to characterise the diodes:

(i) **I-V measurements.** I-V curves have been studied at 77K using a liquid nitrogen prober in order to determine the zero bias resistance (R_o) and hence the R_oA product for the diodes. Values of R_{max} and the open circuit voltage, V_{CO} are also obtained.

(ii) **Detectivity measurements.** Responsivity and noise measurements have been performed to obtain a $D^*\lambda$ value for the diodes under the following conditions:

Detector temperature	77K
Detector field of view	±30°
Signal frequency	1800 Hz
Noise bandwidth	100 Hz centred on 1800 Hz
Source	600°C black body

(iii) **Spectral response measurements.** The spectral responsivity of the diodes has been measured to determine their cut-off wavelength, λ_{CO}, and hence bandgap Eg. The spectral measurement also provides a check on x values and compositional uniformity of the layers and can be compared with transmission measurements (FTIR) performed on the layers prior to processing.

(iv) **Optical beam induced current mapping (OBIC) and electron beam induced current mapping (EBIC).** These techniques have been used to determine the actual sensitive area of the diodes and the location of the junction within the layer. OBIC maps were obtained using a scanned infrared beam at 4 μm.

2.2.2 Results and discussion

(a) MWIR

Results from MWIR diodes fabricated in both (100) and (111)MCT/(100)GaAs were reported last year [8,17]. Results from LWIR diodes fabricated in (100)MCT/(100) GaAs will be reported at the IEE Conference on Advanced Infrared Detectors and Systems, London, June, 1990 [18]. The results are summarised in Table 10. Typical I-V curves, OBIC mappings and spectral curves are shown as Figures 3-5 (λ_{CO} = 3.9 μm) 6-8 (λ_{CO} = 7.6 μm) and 9-11 (λ_{CO} = 10.6 μm).

(i) 77K R_0A versus cut-off wavelength

A plot of 77K R_0A values from this work versus cut-off wavelength is shown as Figure 12. This figure shows that the 77K R_0A products are comparable with those obtained on MOCVD MCT/CdTe [18,19,20], MOCVD MCT/CdTe/GaAs/Si [21], LPE MCT/CdZnTe/GaAs/Si [12] and MBE MCT/CZT [6]. Also see section 2.2.2(vi).

(ii) Detectivity

Typical 77K detectivities of 1.5×10^{11} cmHz$^{1/2}$w^{-1} and 1.1×10^{11} cmHz$^{1/2}$w^{-1} have been obtained for 77K 5.5 and 11 μm cut-off diodes respectively with quantum efficiencies greater than 70%. These results are as good as the best obtained on THM material.

At higher temperatures the detectivity of the MOCVD diodes is better than that obtained in THM material, for example, at 193K the detectivity of the 5.5 μm cut-off diode was 1.3×10^{10} cm $Hz^{1/2}W^{-1}$ - see conclusions.

(iii) Sensitive Area

The OBIC mappings (Figures 4 and 7) show that the sensitive area is smaller than the mask geometry (60 x 100 μm^2 in these cases). This is thought to be due to the high sheet resistance of the diffused 'n' region which reduces the carrier collection efficiency away from the n contact. An ion implantation step was performed to produce a thin n^+ region to decrease the resistance. Figures 10 and 13 are OBIC maps of ion-implanted/diffused diodes which demonstrate a much more uniform sensitive area. The following experiment was performed to establish that the ion implantation step did not in itself form the p-n junction. Layer 1251 (1) was divided into two pieces, one half ion implanted and diffused, and one half ion implanted only. Very good results were obtained in the ion implanted/diffused half but no diode action was seen in the implanted half.

The I-V characteristics of the implanted/diffused diodes are inferior to those of the diffused only devices, in terms of a lower R_oA, or a low reverse bias breakdown voltage. It is important to optimise the diffusion/implantation conditions to maximise the diode performance and the sensitive area.

(iv) Yield

The yields have been estimated by measuring I-V characteristics of the linear arrays. In the (100) orientation 125 and 95 diodes were measured and the yields were 77 and 68%. However most of the defects were due to hillocks and if the diodes fabricated on hillock regions were omitted from the measurement, the estimated yield becomes approximately 95%. The yield on (111)MCT with its smooth surface morphology was 90%.

(v) Substrate orientation studies

It was shown in the first year's annual report that p to n conversion by mercury diffusion is slower on (100)MCT than on (111) epilayers and also that the junction is more homogeneous in the (100)MCT. This could be due to the presence of twinning in the (111) layers which may give rise to areas of high recombination at the twin boundaries. However the (100) layers have a hillocked morphology which causes processing problems and leads to a lower yield of good diodes than on the smooth (111) layers.

(vi) Variation of R_0 with temperature

The variation of the zero bias resistance R_0 for a 12.1 μm cut-off diode versus 1000/T is shown in Figure 14. The linear part, which indicates a diffusion limited current mechanism, extends down to 90K. Below this temperature the curves deviate with a monotonically decreasing slope probably caused by a tunnelling process. Similar studies have been made by DeWames, Arias et al [22] and [6] on LPE/bulk heterojunctions and MBE

HgCdTe/GaAs though with λ_{co} (80K) in the range 8 to 9 μm. At temperatures below 65K they conclude from forward bias measurements that the current generation mechanism is thermally assisted tunnelling originating from defects. The present results are consistent with this.

On LPE layers (with CdZnTe substrates) Destefanis [23] reports a diffusion limited behaviour down to a lower temperature of 70K, while tunnelling dominates at still lower temperatures.

Figure 15 shows the variation of the R_oA product with energy gap at 77K in the range of λ_{co} from 7 to 13 μm for diodes produced on MCT/GaAs and on bulk THM material [20]. The two straight lines indicate the range of SAT's commonly achieved bulk results. The λ_{co} = 12.1 μm 77K THM R_oA value is comparable to that for the equivalent MOCVD point in Figure 14. There is a lower reverse bias breakdown observed in these MOCVD diodes compared to THM diodes. There is no evidence of a generation-recombination dominated region, and so an improvement in the 77K performance might be achieved with optimisation of processing.

At the higher temperature (140K) the MOCVD diodes exhibit a much higher R_oA product than the equivalent THM diodes. This is due to the high diffusion currents which limit the performance of the THM diodes.

Conclusions

State-of-the-art MWIR and LWIR diodes have been fabricated in both (111) and (100)MCT on GaAs with a variety of buffers. In some cases the MOCVD

material behaves very differently from THM material, so it was necessary to investigate the annealing behaviour in order to understand the diffusion mechanism within the material.

The performance of the MOCVD diodes is as good as that of THM diodes at 77K. At higher temperature the performance of the MOCVD diodes is significantly better than that of the THM diodes (as shown by the R_0A and detectivities).

This demonstration of high quality LWIR and MWIR diode arrays in MCT/GaAs is an important first step towards integration with readout circuitry formed in the growth substrate.

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Table 1: MCT/CdTe layers submitted for device processing

Sample No.	MCT orientation	x	MCT thickness (μm)	Hall results (77K,0.2T)			Status
				n or p	Carrier concentration (cm^{-3})	Mobility (cm^2/Vs)	
661	(111)	0.274	6.8	p	5×10^{16}	130	Sample considered too small to be processed
664	(111)	0.268	6.8	p	3×10^{16}	280	Good LWIR diodes fabricated
1035	(111)	0.317	12	p	7×10^{15}	320	Damaged during processing
1044	(111)	0.255	13	p	1×10^{16}	660	60% yield of diodes, some short circuits
1181	(100)	0.211	19.7	*n/p	2×10^{15}	1×10^{4}	Sample considered too small to process (10 mm x 15 mm). Used for annealing experiments
1184	(100)	0.194	19.5	*n/p	4×10^{15}	2×10^{4}	Sample considered too small to process (10 mm x 15 mm). Used for annealing experiments

* mixed conduction - due to presence of HgTe layer

Table 2: The effect of various growth parameters on (100)MCT/CdTe/unetched GaAs

Layer No	Pre-bake temperature (°C)/time (mins)	Nucleation temperature (°C)/time (mins)	Buffer thickness (μm)	Facet density (cm^2)	x	t	Hall	Average FWHM (arc secs)	Comments
1251	630/20	310/22.5	4.2	20-50	0.225	20	classical p	166	Sent to SAT
1252 (1)	630/35	310/20	4.7	10-40	0.228	20.8	classical p	216	Nucleation and buffer annealed
1252 (2)	630/35	310/20	6	40-100	0.244	18.9	classical p	156	Nucleation and buffer annealed
1254 (1)	630/26	310/40	7.5	100-1000	0.210	21.2	classical p	112	Thicker buffer
1256 (1)	None	310/30	-	-	-	-	-	-	No pre-bake mixed orientation growth
1257 (1)	630/30	310/20	2.5	30-100	0.224	19	classical p	86	Sent to SAT
1260 (1)	630/30	310/27	3.8	50-100	0.206	21.7	classical p	155	30 minute post growth anneal
1261 (1)	630/34	310/20	3.8	1000	0.207	23.5	classical p	97	10 minute post growth anneal, sent to SAT
1263 (1)	630/20	310/20	2.5	100-1000	0.214	22.6	classical p	87	Sent to SAT
1264 (1)	630/20	310/20	-	-	-	-	-	-	Mixed orientation growth
1265 (1)	630/32	300/60	2.8	100-1000	0.254	17.4	classical p	150	Sent to SAT
1267 (1)	630/20	300/60	3.3	100-1000	0.247	9.4	anomalous	-	-

Table 3: (111)MCT layers on GaAs supplied to SAT for device processing

Layer No	GaAs substrate orientation	CdTe buffer thickness (μm)	x	MCT thickness (μm)	Status*
1031	(111)	2.5	0.239	14	Damaged during processing
1033	(111)	4	0.335	11	Shorted diffused diodes
1036	(100)	4	0.257	18	Good SWIR diffused diodes made
1296	(111)	3	0.258	18	Annealing experiments
1298	(111)	3	0.252	18	Poor diffused diodes

* See Section 2.2 for further details

Table 4: (100)MCT layers on (100)GaAs supplied to SAT for device processing

Layer No	Buffer type and thickness (μm)	x	MCT thickness (μm)	FWHM (arc secs)	Status* of diffused diodes
1094	6 μm high x MCT	0.3	15	133	Good
1112	5 μm HgTe/0.6 μm CdTe	0.2	12	187	Good
1114	0.4 μm CdTe/2 μm HgTe/0.4 μm CdTe/2 μm HgTe/0.4 μm CdTe	0.2	12	145	Very variable
1124	4 μm/0.6 μm CdTe/4 μm HgTe/0.6 μm CdTe	0.3	15	-	Small area
1125	1 μm CdTe	0.265	11.9	-	Poor
1127	2.5 μm CdTe	0.25	15	-	
1251	4 μm CdTe	0.225	19	143,189	Good
1257 (1)	2.5 μm CdTe	0.224	19	86,86	Good
1261 (1)	3.8 μm CdTe	0.208	23.5	94,99	Poor
1263 (1)	2.5 CdTe	0.212	22.6	85,88	Poor
1265 (1)	2.8 μm CdTe	0.254	17.4	210,89	Poor
1266 (1)	3.8 μm CdTe	0.247	18.4	173,346	Good

* **See Section 2.2 for further details**

Table 5: 77K Hall effect measurements on layer 1114 showing that the sample could be annealed successfully to p-type

		Hall measurements							
			0.1T		0.3T		0.5T		
Sample No	Annealing	Type	Carrier concentration (cm^{-3})	Mobility (cm^2/Vs)	Carrier concentration (cm-3)	Mobility (cm^2/Vs)	Carrier concentration (cm^{-3})	Mobility (cm^2/Vs)	
1114 (1)	As grown	n/p*	4.3 E14	16500	5.8 E14	12200	8.4 E16	8500	
1114 (2)	As grown after Br/methanol etching (4 microns)	n/p*	9.7 E14	4550	1.5 E15	2950	2.3 E15	1900	
1114 (3)	295°C 2 hours under vacuum	p	3.4 E16	260	3.2 E16	285	3.1 E16	292	
1114 (4)	315°C 2 hours under vacuum	p	4.5 E16	320	4.5 E16	325	4.3 E16	335	

* Layer showed mixed conduction

Table 6: 77K Hall effect measurements on layer 1296 showing that the sample could be annealed successfully to p-type (1296 (2) and (3)), and that the n anneal needs further optimisation (1296 (4) and (5))

		Hall measurements							
			0.1T		0.3T		0.5T		
Sample No	Annealing	Type	Carrier concentration (cm^{-3})	Mobility (cm^2/Vs)	Carrier concentration (cm^{-3})	Mobility (cm^2/Vs)	Carrier concentration (cm^{-3})	Mobility (cm^2/Vs)
1296 (1)	As grown	n/p*	6.6 E14	38000	8.0 E14	31400	9.5 E14	37900
1296 (2)	300°C 2 hours under vacuum	p	3.1 E16	320	2.6 E16	380	2.4 E16	405
1296 (3)	300°C 2 hours under vacuum	p	1.9 E16	405	1.7 E16	440	1.7 E16	440
1296 (4)	300°C 2 hours under vacuum followed by 300°C 27 hours under Hg pressure	n/p*	3.7 E15	4300	4.5 E15	3550	5.6 E15	2800
1296 (5)	300°C 2 hours under vacuum followed by 300°C 27 hours under Hg pressure	n/p*	1.2 E16	1200	1.3 E16	1100	1.6 E16	940

* Layer showed mixed conduction

Table 7: 77K Hall effect measurements on layer 1181. The presence of a HgTe buffer layer dominated the Hall measurements

		Hall measurements							
			0.1T		0.3T		0.5T		
Sample No	Annealing	Type	Carrier concentration (cm^{-3})	Mobility (cm^2/Vs)	Carrier concentration (cm^{-3})	Mobility (cm^2/Vs)	Carrier concentration (cm^{-3})	Mobility (cm^2/Vs)
1181 (1)	As grown	n/p*	2.0 E15	15000	7.5 E15	3950	1.2 E16	1500
1181 (2)	315°C 2 hours under vacuum	n/p*	1.6 E15	2400	2.0 E17	190	2.0 E17	200
1181 (2)	315°C 2 hours under vacuum followed by 315°C 4 hours under vacuum	n/p*	3.4 E16	1870	8.1 E16	1152	9.7 E16	956

* Layer showed mixed conduction

Table 8: 77K Hall effect measurements on layer 1184. The presence of a HgTe buffer layer dominated the Hall measurements

		Hall measurements						
			0.1T		0.3T		0.5T	
Sample No	Annealing	Type	Carrier concentration (cm^{-3})	Mobility (cm^2/Vs)	Carrier concentration (cm^{-3})	Mobility (cm^2/Vs)	Carrier concentration (cm^{-3})	Mobility (cm^2/Vs)
1184 (1)	As grown	n/p*	1.1 E15	91500	3.3 E15	31300	7.6 E15	13300
1184 (2)	315°C 2 hours under vacuum	n/p*	6.5 E15	11190	3.7 E16	1980	1.9 E17	390
1184 (2)	315°C 2 hours under vacuum followed by 315°C 4 hours under vacuum	n/p*	5.6 E15	13850	2.8 E16	2760	1.0 E17	715
1184 (3)	315°C 2 hours under vacuum followed by 315°C 4 hours under vacuum	n/p*	1.9 E16	2590	1.8 E17	265	4.3 E17	114

* Layer showed mixed orientation

Table 9: 77K Hall effect measurements on layer 1257

		Hall measurements							
			0.1T		0.3T		0.5T		
Sample No	Annealing	Type	Carrier concentration (cm^{-3})	Mobility (cm^2/Vs)	Carrier concentration (cm^{-3})	Mobility (cm^2/Vs)	Carrier concentration (cm^{-3})	Mobility (cm^2/Vs)	
1257 (1)	As grown	p	8.5 E16	190	4.7 E16	350	4.2 E16	390	
1257 (2)	210°C 6 days under Hg pressure	n/p*	3.5 E14	22900	5.5 E14	13500	1.5 E15	6900	
1257 (3)	300°C 24 hours under Hg pressure	n/p*	3.5 E14	15700	5.8 E14	10500	8.8 E14	6300	

* Layer showed mixed conduction

Table 10: MWIR and LWIR photodiode results in MOCVD CMT/GaAs (100)

Layer No	MCT orientation and thickness (μm)	Buffer structure	77K λ_{co} (μm)	R_oA at 77K (Ωcm^2)
1094	(100), 16	6 μm high x CMT/1.5 μm CdTe	3.9	9.4×10^4
1123	(100), 16	5 μm HgTe/2 μm CdTe	5.7	1.4×10^4
1306C	(111), 18	3 μm CdTe	5.7	3.4×10^4
1036D	(111), 18	3 μm CdTe	5.9	3.2×10^3
1112	(100), 16	5 μm/0.6 μm CdTe	6.2	3.8×10^3
1114	(100), 18	0.4 μm CdTe/3 μm HgTe/0.4 μm CdTe/3μm HgTe/0.4 μm CdTe	7.4	474
1036B	(111), 18	3 μm CdTe	7.4	1800
1036A	(111), 18	3 μm CdTe	7.5	454
1036E	(111), 18	3 μm CdTe	7.6	2700
1251A	(111), 19	3 μm CdTe	10.7	12.8
1257	(100), 19	1 μm CdTe	11.0	12
1251B	(100), 19	3 μm CdTe	12.1	2

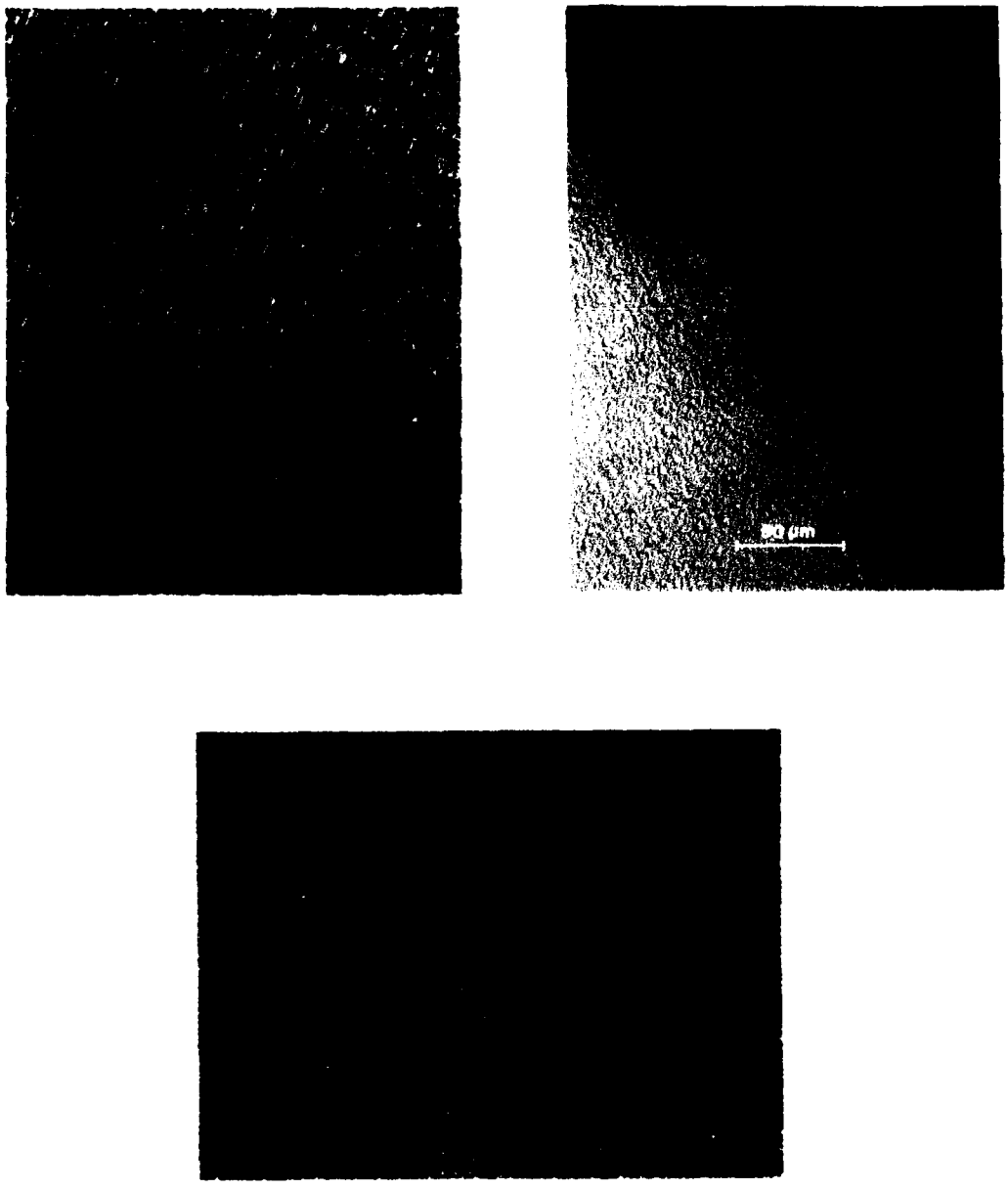


Figure 1: Different surface morphologies obtained of CdTe/(311)GaAs

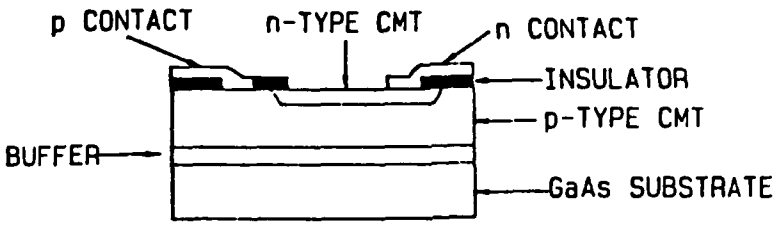


Figure 2: Schematic diagram of photodiode structure used

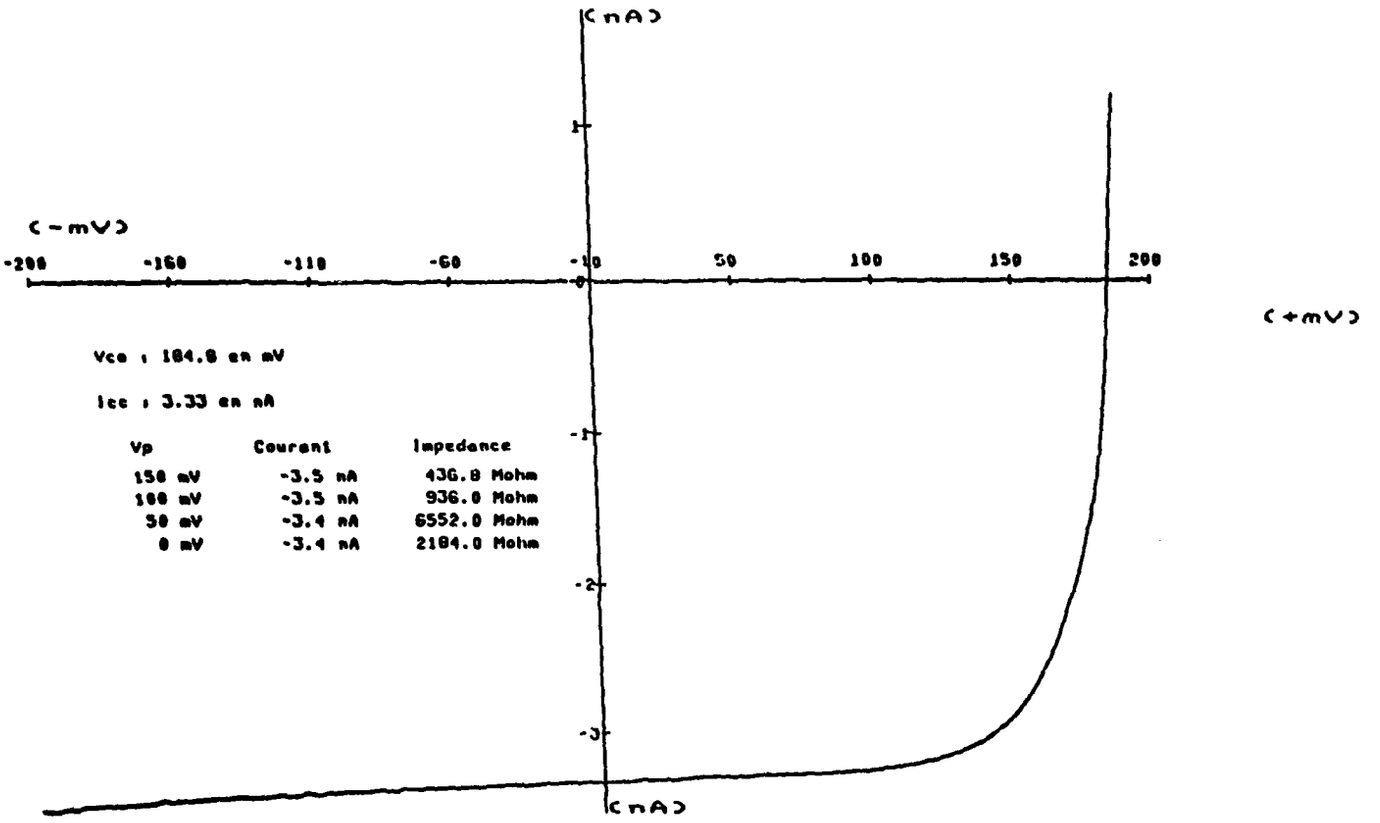
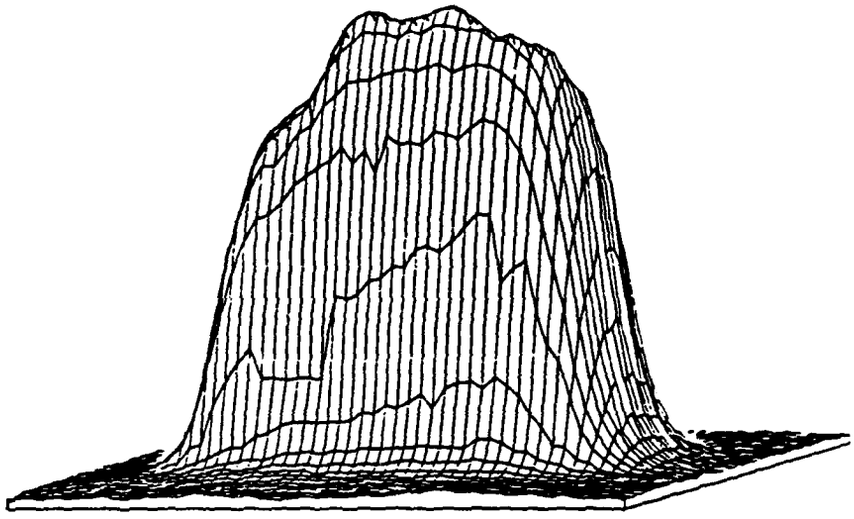


Figure 3: 77K I-V characteristic of a diode from layer 1094



TRACE EN PERSPECTIVE

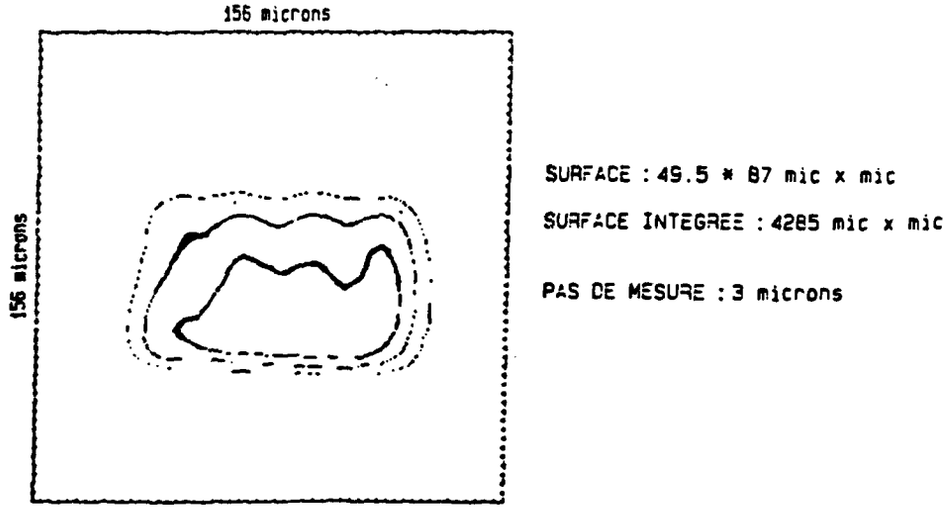


Figure 4: OBIC map of a diffused diode from layer 1094

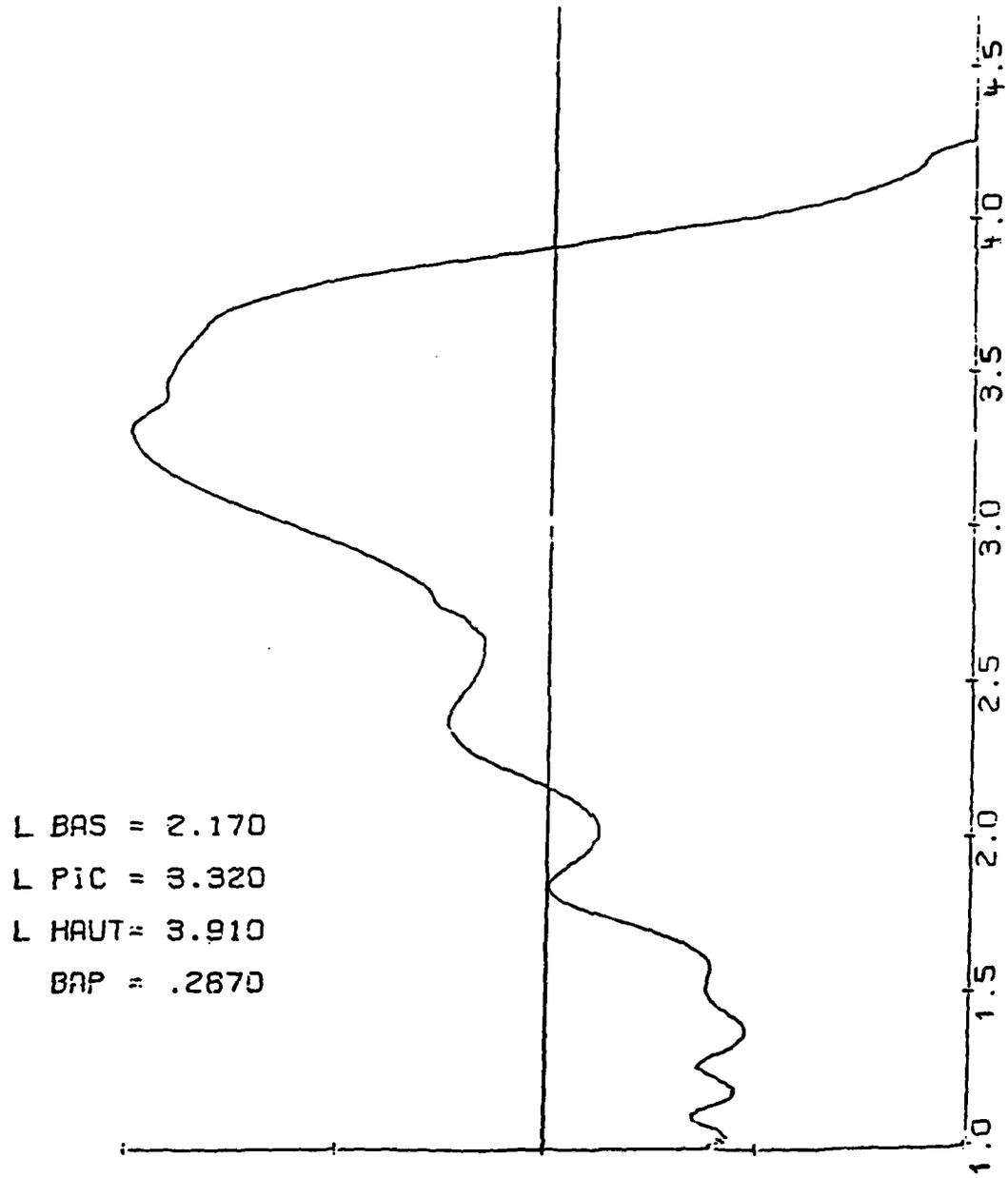


Figure 5: Spectral response from a diode from layer 1094

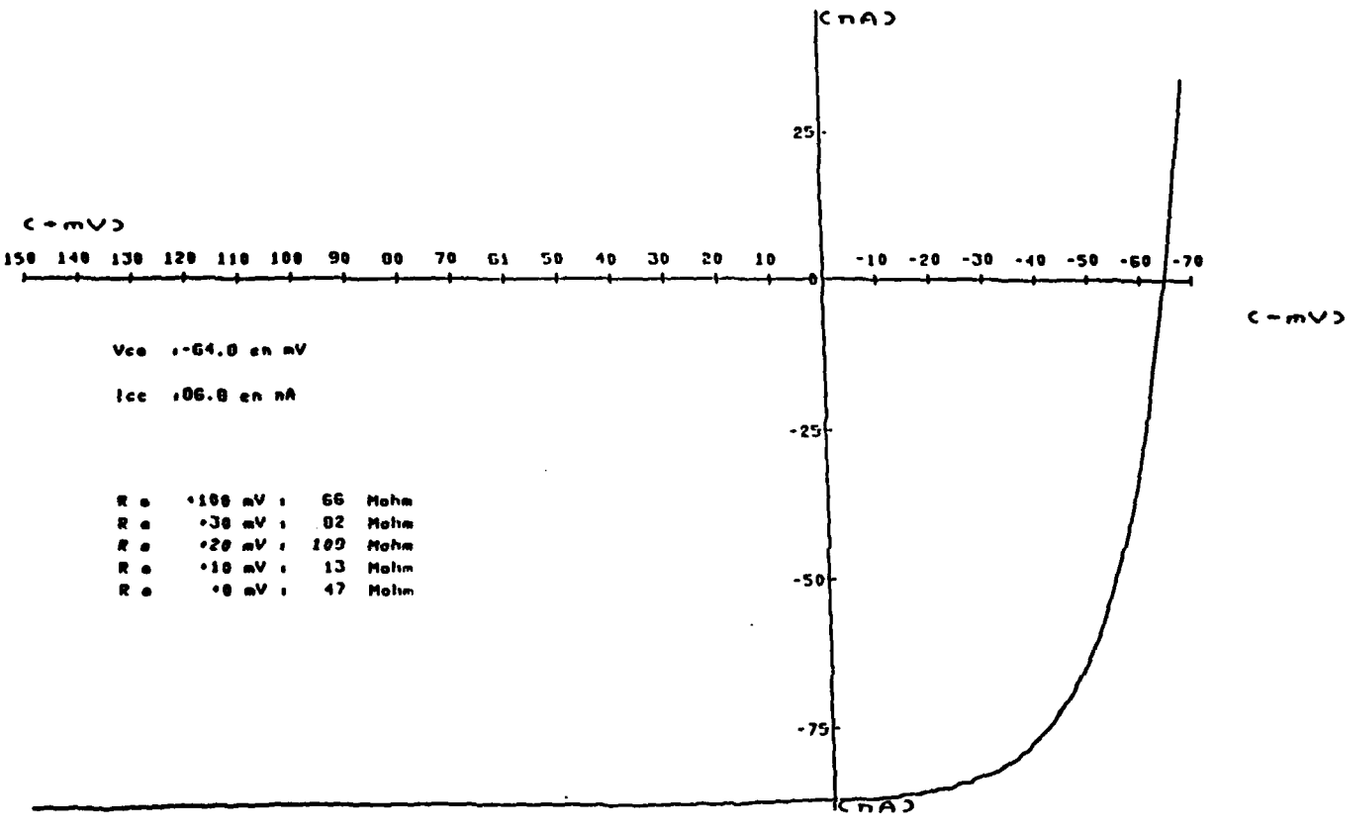
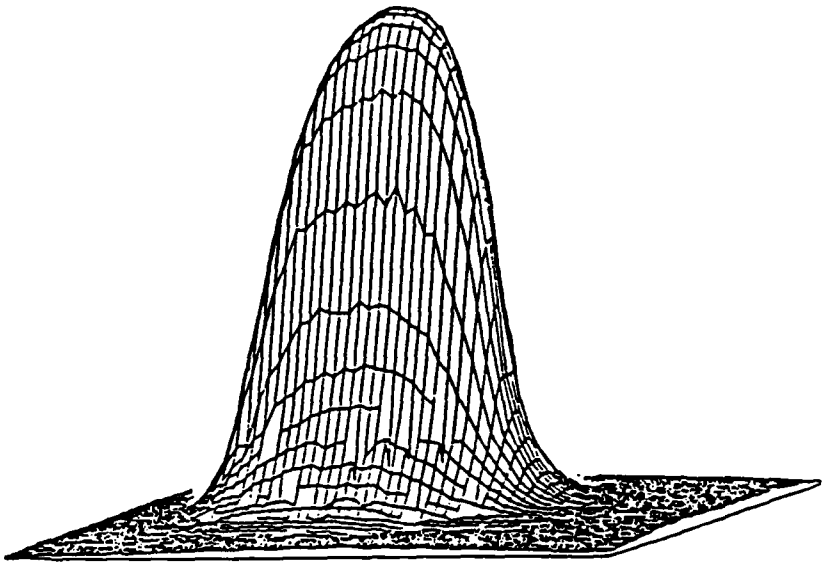
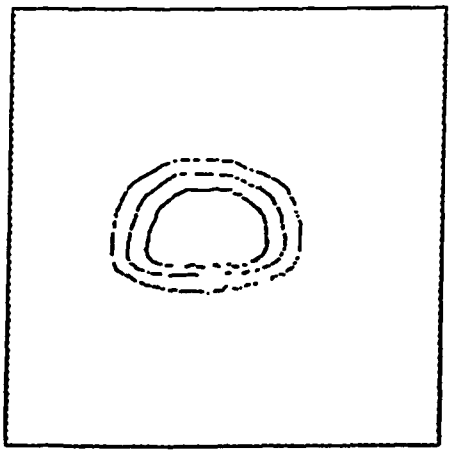


Figure 6: 77K I-V characteristic of a diode from layer 1036



TRACE EN PERSPECTIVE

SURFACE : 42 x 65
SURFACE INTEGREE : 3244



COURBES DE NIVEAUX :75%-50%-25%
PAS DE MESURE : 3 microns

Figure 7: OBIC map of a diode from layer 1036

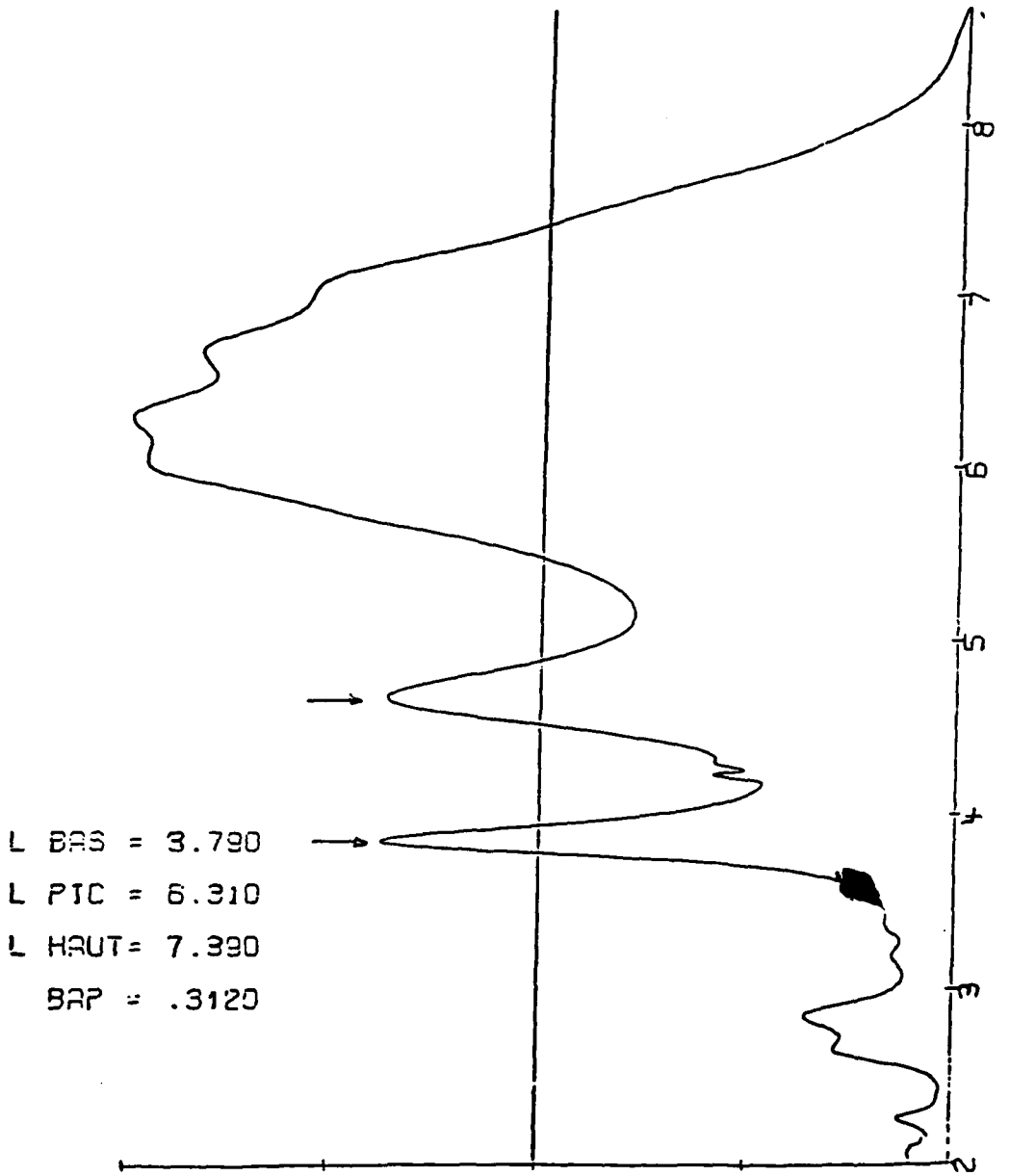


Figure 8: Spectral response of a diode from layer 1036

The two peaks indicated by arrows are due to anomalous transmission through the dewar window

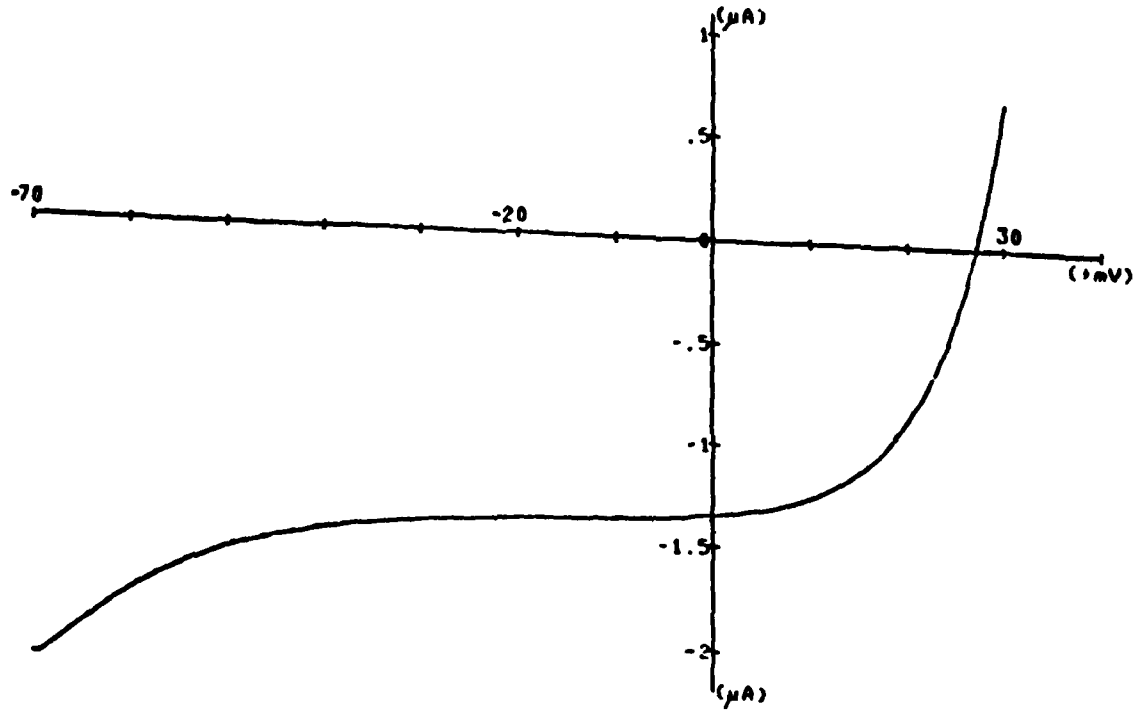
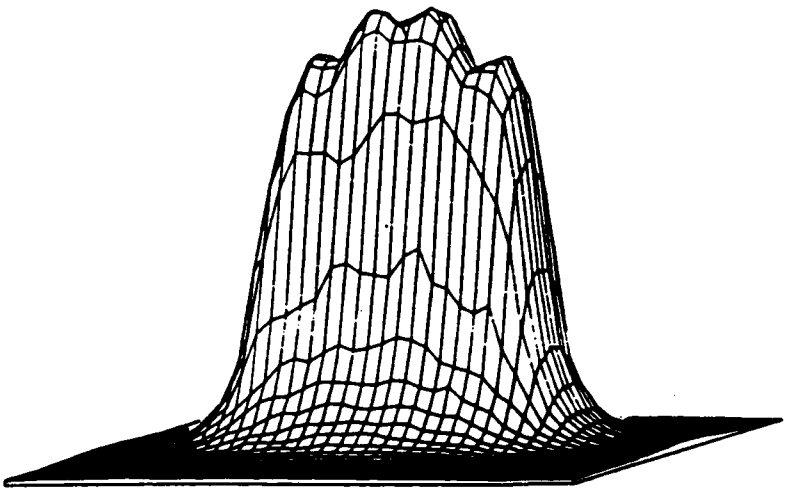


Figure 9: I-V characteristic of a diode from layer 1251



TRACE EN PERSPECTIVE

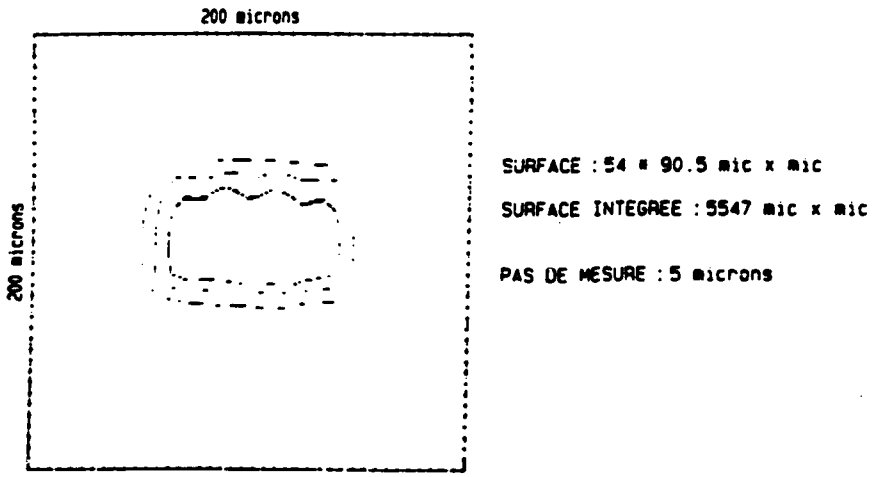
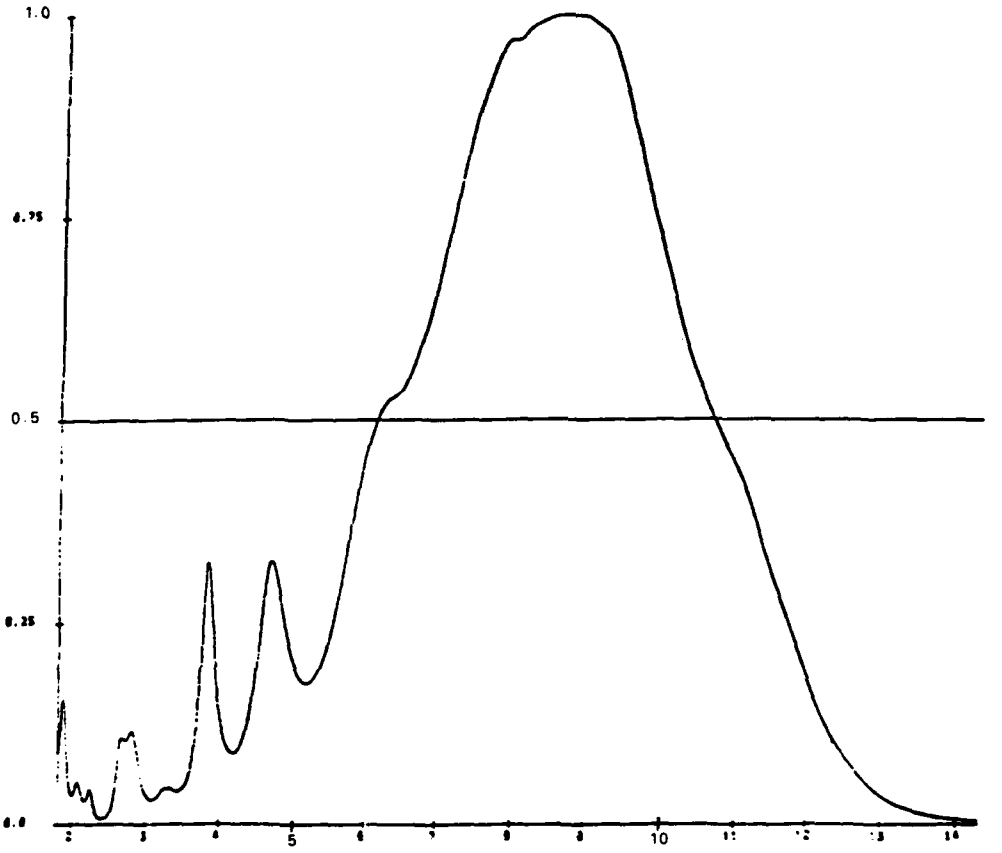


Figure 10: OBIC map of an implanted and diffused diode from layer 1251



L BAS = 5.12 UM

L PIC = 8.79 UM

L HAUT = 10.57 UM

BAP = 0.296

Figure 11: Spectral response of a diode from wafer 1251

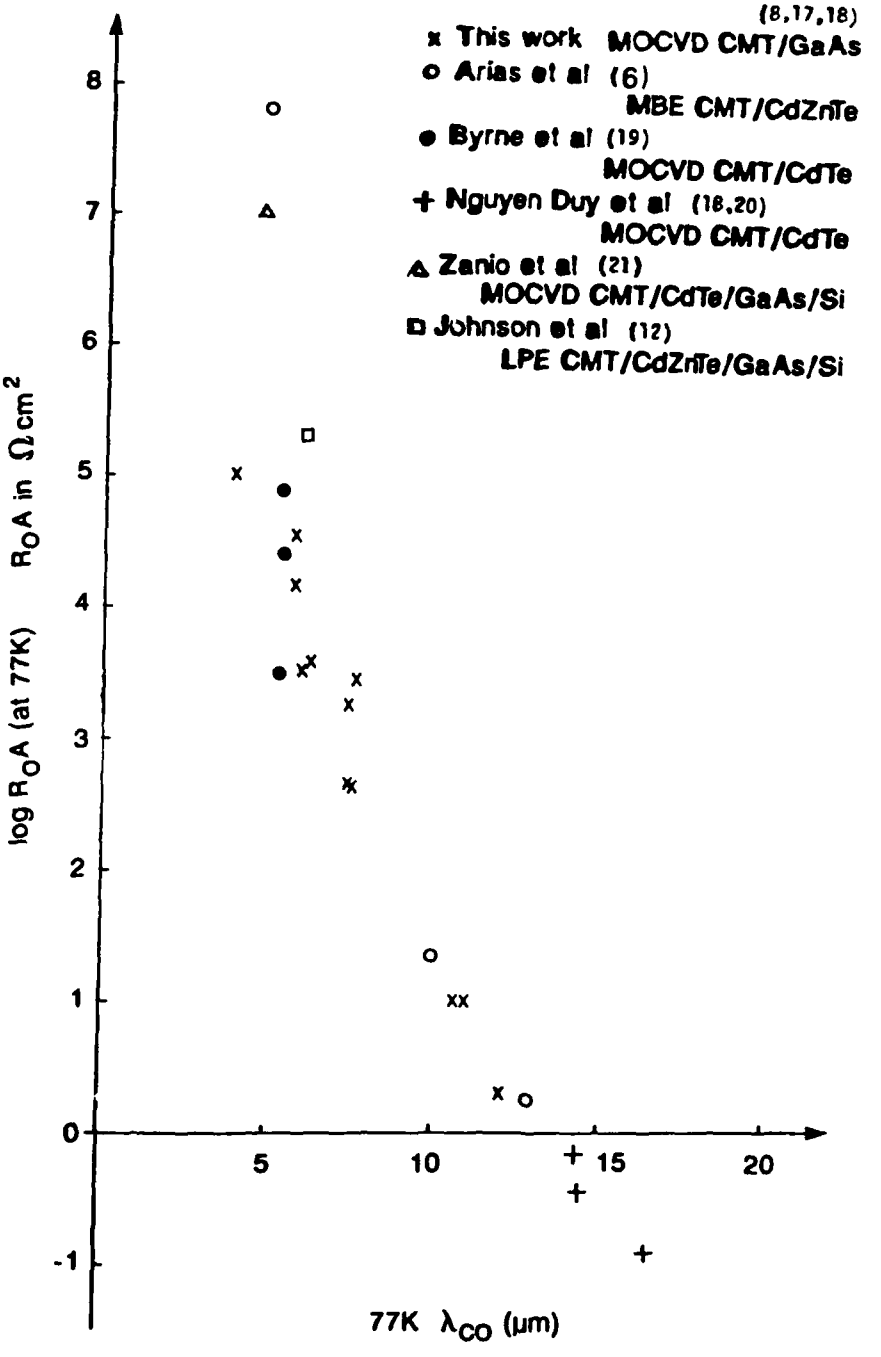
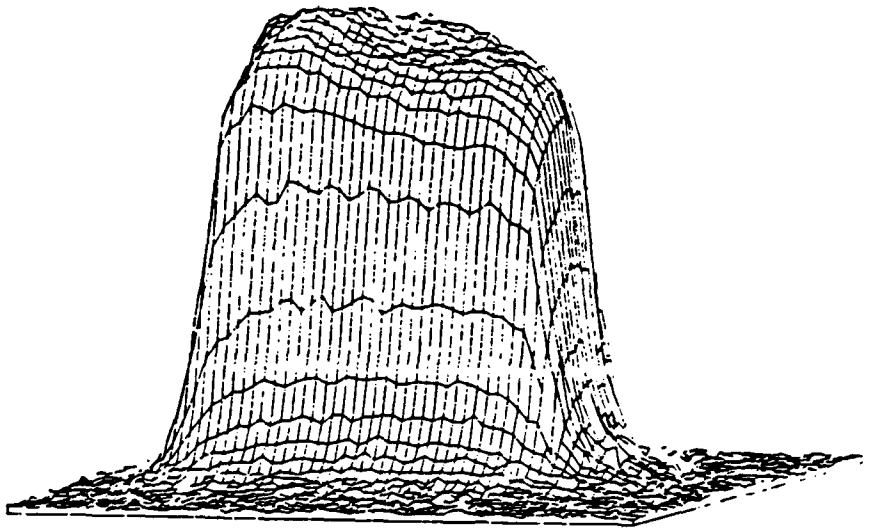


Figure 12: 77K R_OA values versus 77K cut-off wavelength



TRACE EN PERSPECTIVE

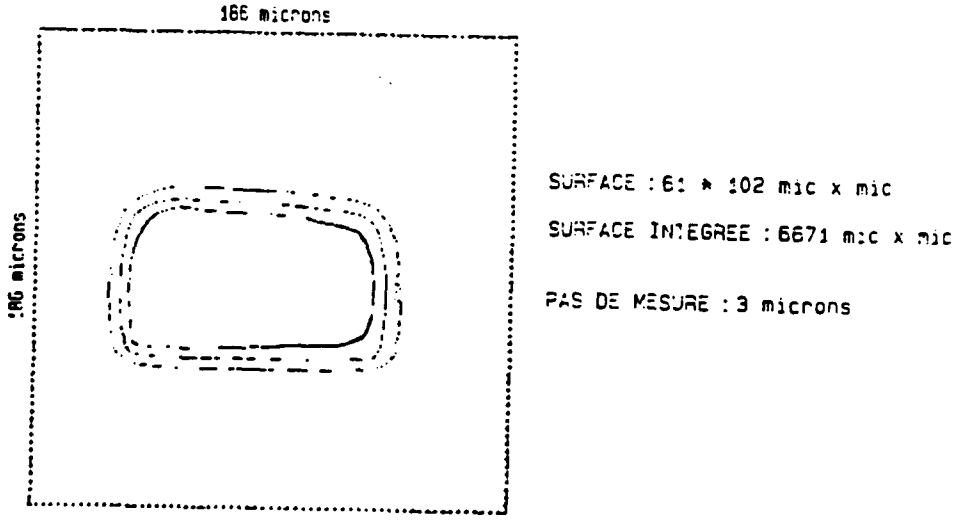


Figure 13: OBIC map of an ion implanted and diffused diode from layer 1125 showing a more uniform sensitive area

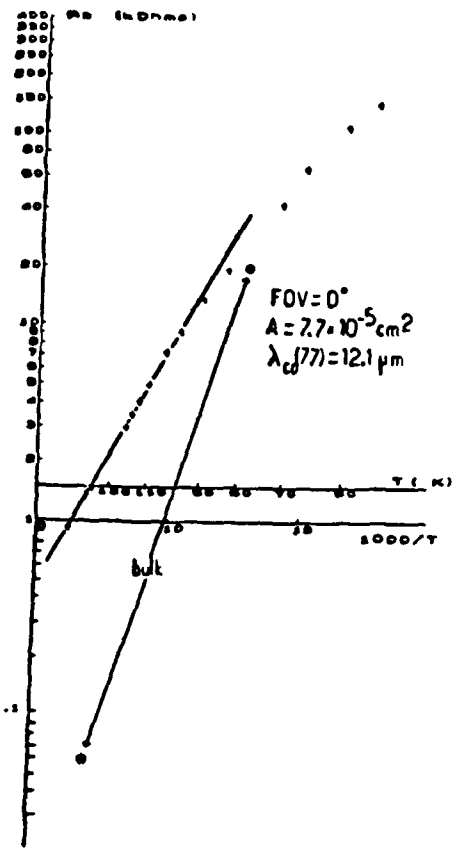


Figure 14: Zero bias resistance versus 1000/T for 12.1 μm cut-off diodes in MOCVD MCT/GaAs and bulk MCT

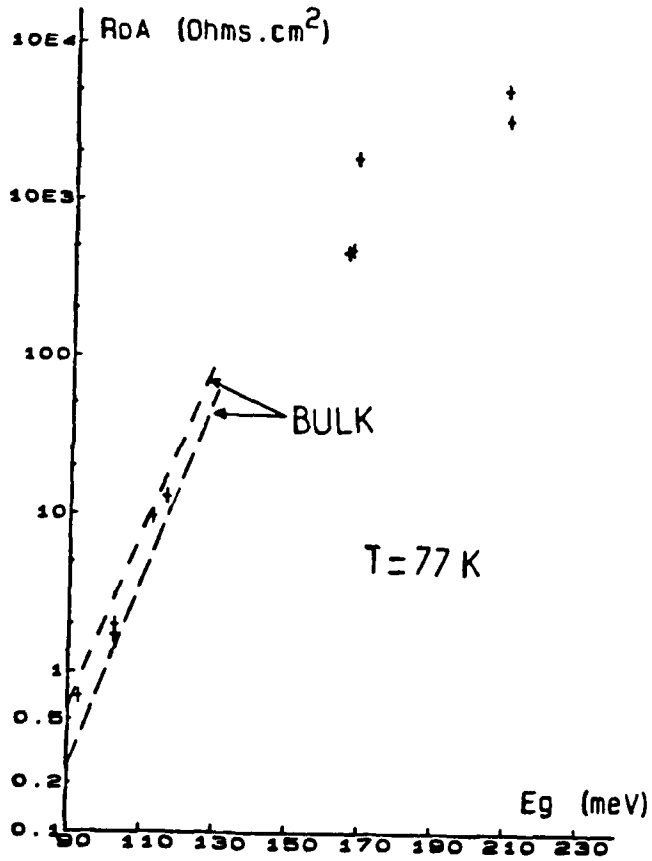


Figure 15: 77K R_0A versus energy bandgap of LWIR diodes in MCT/GaAs, with a comparison to diodes in SAT bulk MCT